CLAIMS

What is claimed is:

1. A memory system architecture comprising:

a memory controller;

a plurality of memory modules, each memory module containing a plurality of memory chips;

a command and address bus coupling the memory controller to each of the plurality of memory modules such that a command and address signal propagated from the memory controller to one of the memory chips is propagated serially to each of the plurality of memory modules, the command and address signal divided into two or more components at each memory module, each component corresponding to a group of memory chips of a respective memory module, each component propagated serially to each of the memory chips of the corresponding group of memory chips.

2. The memory system architecture of claim 1 wherein the two or more components of the command and address signal are recombined after propagation through each of the memory chips of the respective memory module prior to propagation to a subsequent memory module of the plurality of memory modules.

3. The memory system architecture of claim 2 wherein the command and address signal is terminated upon propagation through each memory chip of each of the plurality of memory modules.

4. The memory system architecture of claim 1 wherein each memory module is a dual in-line memory module and each memory chip is a dynamic random access memory chip.

5. The memory system architecture of claim 2 wherein the command and address bus is a unidirectional address bus.

6. The memory system architecture of claim 3 wherein the plurality of memory modules comprises two memory modules and the plurality of memory chips comprises sixteen memory chips.

7. The memory system architecture of claim 6 wherein the command and address signal is terminated at a signal termination point on a final memory module after propagating serially through each of the plurality of memory modules.

8. The memory system architecture of claim 6 wherein a first impedance between a connector on the chipset and a connector on the first memory module is less than a second impedance through a memory module.

9. The memory system architecture of claim 8 wherein the second impedance is the same, within a specified tolerance, as a third impedance through the plurality of memory chips plus a Bloch mode impedance corresponding to a specified data output frequency.

10. The memory system architecture of claim 9 wherein a chipset driver impedance is the same, within a specified tolerance, as the first impedance and an impedance of the signal termination point is the same, within a specified tolerance, as the second impedance.

11. A method comprising:

propagating a command and address signal from a chipset over a command and address bus to one of a plurality of memory modules, each memory module containing two or more groups of memory devices;

dividing the command and address signal into a plurality of components, each component corresponding to a group of memory devices of a respective memory module;

propagating each component serially, to each of the memory devices of the corresponding group of memory devices.

12. The method of claim 11 further comprising:

recombining the plurality of components of the command and address signal after propagation through each of the memory devices of the corresponding group of memory devices; and

propagating the recombined command and address signal to a subsequent memory module of the plurality of memory modules.

13. The method of claim 12 wherein the command and address signal is terminated upon propagation through each memory device of each of the plurality of memory modules.

14. The method of claim 11 wherein each memory module is a dual in-line memory module and each memory device is a dynamic random access memory device.

15. The method of claim 12 wherein the command and address bus is a unidirectional address bus.

16. The method of claim 11 wherein the plurality of memory modules comprises two memory modules and the plurality of memory devices comprises sixteen memory devices.

17. The method of claim 16 further comprising:

terminating the command and address signal at a signal termination point on a final memory module after propagating serially through each of the plurality of memory modules.

18. The method of claim 16 wherein a first impedance between a connector on the chipset and a connector on the first memory module is less than a second impedance through a memory module.

19. The method of claim 18 wherein the second impedance is the same, within a specified tolerance, as a third impedance through the plurality of memory devices plus a Bloch mode impedance corresponding to a specified data output frequency.

20. The method of claim 19 wherein a chipset driver impedance is the same, within a specified tolerance, as the first impedance and an impedance of the signal termination point is the same, within a specified tolerance, as the second impedance.

21. A system comprising:

a processor;

a memory controller coupled to the processor;

a command and address bus coupled to the memory controller, the command and address bus configured to propagate a command and address signal to one of a plurality of memory modules, divide the command and address signal into a plurality of components, each component corresponding to a particular group of memory devices of a plurality of memory devices contained on the memory module, and propagate each component serially to each of the memory devices of the corresponding group of memory devices.

22. The memory system architecture of claim 21 wherein the plurality of components of the command and address signal are recombined after propagation through each of the memory devices of the memory module prior to propagation to a subsequent memory module of the plurality of memory modules.

23. The memory system architecture of claim 22 wherein the command and address signal is terminated upon propagation through each memory device of each of the plurality of memory modules.

24. The system of claim 21 wherein each memory module is a dual in-line memory module and each memory device is a dynamic random access memory device.

25. The system of claim 21 wherein the command and address bus is a unidirectional address bus.

26. The system of claim 21 wherein the plurality of memory modules comprises two memory modules and the plurality of memory devices comprises sixteen memory devices.

27. The system of claim 26 further comprising:

terminating the command and address signal at a signal termination point on a final memory module after propagating serially through each of the plurality of memory modules.

28. The system of claim 26 wherein a first impedance between a connector on the memory controller and a connector on the first memory module is less than a second impedance through a memory module.

29. The system of claim 28 wherein the second impedance is the same, within a specified tolerance, as a third impedance through the plurality of memory devices plus a Bloch mode impedance corresponding to a specified data output frequency.

30. The system of claim 29 wherein a memory controller driver impedance is the same, within a specified tolerance, as the first impedance and an impedance of the signal termination point is the same, within a specified tolerance, as the second impedance.